IN THE CLAIMS

Please amend the claims as follows where a copy of the claims with the amendments delineated are set forth below in accordance with the PTO guidelines. This listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Currently Amended) ~~The method according to claim 5, wherein the step of adding the articulated fan-in driving the signal to the analysis region comprises~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. manually modifying the analysis region if verification of the circuit design over the analysis region results in false including the steps of:

1. selecting a signal in the analysis region; and

2. adding a portion of the circuit design relating to the signal in the analysis region including adding the articulated fan-in driving the signal to the analysis region by identifying the articulated fan-in of the signal by traversing the circuit design backwards from the signal until a signal from the group consisting of~~:~~ primary inputs, storage

elements and articulation points is encountered.

7. (Cancelled)

8. (Currently Amended) ~~The method according to claim 7, wherein the step of adding a portion of the articulated fan-in driving the signal to the analysis region comprises.~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. manually modifying the analysis region if verification of the circuit design over the analysis region results in false including the steps of:

1. selecting a signal in the analysis region; and

2. adding a portion of the circuit design relating to the signal in the analysis region having the step of adding a portion of an articulated fan-in driving the signal to the analysis region including adding a portion of the articulated fan-in driving the selected signal that is ~~'turned on'~~ turned-on by current value assignments in the Plot window to the analysis region; and

repeating steps b-c until the circuit design is verified or until a user identifies an error in the circuit design

9. (Currently Amended) ~~The method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. manually modifying the analysis region if verification of the circuit design over the analysis region results in false including the steps of:

1. ~~a.~~ selecting a signal in the Plot window ~~at time cycle just after the circuit design~~

~~is reset~~; and

2. ~~b.~~ adding the reset portion of ~~the~~ an articulated fan-in of the selected signal in the analysis region; and

repeating steps b-c until the circuit design is verified or until a user identifies an error in the circuit design.

10. (Cancelled)

11. (Currently Amended) ~~The method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. manually modifying the analysis region if verification of the circuit design over the analysis region results in false including the steps of:

1. ~~a.~~ the user selecting an articulation point inside the analysis region; and

2. ~~b.~~ removing ~~the~~ an articulated fan-in of the articulation point from the analysis region and/or adding the articulated fan-in driving the selected articulation point to the analysis region; and

repeating steps b-c until the circuit design is verified or until a user identifies an error in the circuit design.

12. (Cancelled)

13. (Currently Amended) ~~The method according to claim 1, wherein manually modifying the analysis comprises the steps of:~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. manually modifying the analysis region if verification of the circuit design over the analysis region results in false including the steps of:

1. a. the user selecting at least one signal in the analysis region from the Plot window, wherein each signal is selected at a specific time cycle;

2. b. generating a triple based on each selected signal, wherein a triple comprises the name of the selected signal, the specific time cycle of selection and the value of the selected signal at the specific time cycle;

3. c. generating a rule based on the triples;

4. d. verifying the rule separately; and

5. e. verifying the circuit design using the rule as an assumption for the analysis region;

repeating steps b-c until the circuit design is verified or until a user identifies an error in the circuit design.

14. (Original) The method according to claim 13, wherein the rule is automatically modified in case the step of verifying of the rule results in non-verification.

15. (Cancelled)

16. (Currently Amended) ~~The method according to claim 15, wherein the step of identifying the candidate signals for modification of the analysis region if verification of the circuit design is false comprises~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false including the step of identifying articulation points corresponding to the analysis region as the candidate signals;

d. automatically modifying the analysis region using the candidate signals; and

e. manually modifying the analysis region if there are no appropriate candidate signals; and

repeating steps b-e until the circuit design is verified or until a user identifies an error in the circuit design.

17. (Original) The method according to claim 16, wherein the step of automatically identifying articulation points corresponding to the analysis region comprises the steps of:

a. identifying comparison statements on wide signals as articulation points; and

b. identifying Boolean guards of conditional statements as articulation points.

18. (Currently Amended) ~~The method according to claim 15, wherein the step of automatically modifying the analysis region using the candidate signals include~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false;

d. automatically modifying the analysis region using the candidate signals including the step of prioritizing the candidate signals on the basis of productivity choices; and

e. manually modifying the analysis region if there are no appropriate candidate signals; and

repeating steps b-e until the circuit design is verified or until a user identifies an error in the circuit design.

19. (Original) The method according to claim 18, wherein the step of prioritizing candidate signals on the basis of productivity choices comprises the steps of:

a. assigning productivity weights to analysis region modification choices;

b. ranking the choices according to the productivity weights wherein the choices with positive productivity weights are considered as high-productivity choices and the choices with negative weights are considered low-productivity choices; and

c. identifying the highest-productivity choices from the high-productivity choices.

20. (Currently Amended) ~~The method according to claim 15, wherein the step of automatically modifying the analysis region comprises.~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false;

d. automatically modifying the analysis region using the candidate signals including at least one of the steps of:

1. expanding the analysis region by including ~~the~~ an articulated fan-in corresponding to the highest-productivity choices that are located at the boundary of the analysis region, and

2. removing the articulated fan-in corresponding to the highest-productivity choices that are located inside the analysis region from the analysis region; and

e. manually modifying the analysis region if there are no appropriate candidate signals; and

repeating steps b-e until the circuit design is verified or until a user identifies an error in the circuit design.

21. (Cancelled)

22. (Original) The method according to claim 18, wherein the step of automatically modifying the analysis region comprises modifying the analysis region using low-productivity choices on the user's decision in case there are no high-productivity choices.

23. (Currently Amended) ~~The method according to claim 15, wherein the step of manually modifying analysis if there are no appropriate candidate signals, comprises the steps of:~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method

comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false;

d. automatically modifying the analysis region using the candidate signals; and

e. manually modifying the analysis region if there are no appropriate candidate signals including the steps of:

1. ~~a.~~ defining an abstraction created in response to the low productivity choices in the analysis region;

2. ~~b.~~ proving the abstraction in the circuit design separately; and

3. ~~c.~~ verifying the circuit design using the abstraction in the analysis region; and

repeating steps b-e until the circuit design is verified or until a user identifies an error in the circuit design.

24. (Original) The method according to claim 23, wherein the step of defining an abstraction comprises adding new logic to the circuit design corresponding to the abstraction.

25. (Currently Amended) ~~The method according to claim 15, wherein the step of manually modifying the analysis if there are no appropriate candidate signals, comprises the steps of:~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false;

d. automatically modifying the analysis region using the candidate signals; and

e. manually modifying the analysis region if there are no appropriate candidate signals including the steps of:

1. ~~a.~~ defining an assumption created in response to low productivity choices in the analysis region;

2. ~~b.~~ proving the assumption in the circuit design separately; and

3. ~~c.~~ verifying the circuit design using the assumption in the analysis region; and

repeating steps b-e until the circuit design is verified or until a user identifies an error in the circuit design.

26. (Currently Amended) ~~The method according to claim 15, wherein the step of manually modifying the analysis includes the steps of:~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false;

d. automatically modifying the analysis region using the candidate signals; and

e. manually modifying the analysis region if there are no appropriate candidate signals including the steps of:

1. ~~a.~~ the user selecting at least one signal in the analysis region from a Plot window, wherein each signal is selected at a specific time cycle;

2. ~~b.~~ generating a triple based on each selected signals, wherein a triple comprises the name of the selected signal, specific time cycle of selection and the value of the selected signal at the specific time cycle; and

3. ~~c.~~ generating a rule based on the triples;

4. ~~d.~~ verifying the rule separately; and

5. ~~e.~~ verifying the circuit design using the rule as an assumption for the analysis region; and

repeating steps b-e until the circuit design is verified or until a user identifies an error in the circuit design.

27. (Currently Amended) The method according to claim 26, wherein the rule is

automatically modified in case the step of verifying of the rule results in a determination that the analysis region is not verified ~~in a false~~.

28. (Currently Amended) ~~The method according to claim 15, wherein the step of manually verifying the circuit design by applying formal verification over the analysis region comprises~~ A method for guiding formal verification for a circuit design in circuit simulation software to optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region including having a user deciding that there is an error in the circuit design in case there are no high- productivity choices;

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false;

d. automatically modifying the analysis region using the candidate signals; and

e. manually modifying the analysis region if there are no appropriate candidate signals; and

repeating steps b-e until the circuit design is verified or until a user identifies an error in the circuit design.

29. (Currently Amended) A method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for the verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design;

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying articulation points corresponding to the analysis region as analysis region modification choices;

d. automatically modifying the analysis region using ~~the~~ an articulated fan-in of the analysis region modification choices if verification of the digital design over the analysis region results in a determination that the analysis region is not verified ~~in a false~~;

repeating steps b-d until the circuit design is verified; and

repeating steps b-d until a user identifies an error in the circuit design.

30. (Cancelled)

31. (Currently Amended) ~~The system according to claim 30, wherein the system for guiding formal verification of a circuit design to optimize time required for verification process further comprises~~ A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules; and

d. a Productivity Choice Determination tool to determine high-productivity choices for expanding the analysis region if verification fails.

32. (Currently Amended) ~~The system according to claim 30, wherein the system for guiding formal verification of a circuit design to optimize the time required for verification process further comprises~~ A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules; and

d. an Articulation Point Selection tool to identify articulation points corresponding to the analysis region to choose smaller analysis region for circuit verification.

33. (Currently Amended) ~~The system according to claim 30, wherein the system for~~

~~guiding formal verification of a circuit design to optimize time required for verification process further comprises~~ A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules; and

d. a Rule Verifier for verifying user defined rules for the analysis region.

34. (Currently Amended) ~~The system according to claim 30, wherein the system for guiding formal verification of a circuit design to optimize time required for verification process further comprises~~ A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules; and

d. a database for storing a set of triples based on a set of signals selected by the user.

35. (Currently Amended) ~~The system according to claim 30, wherein the GUI comprises~~ A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information including a Source Code window for enabling the user to select a signal from a source code displayed;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules.

36. (Currently Amended) ~~The system according to claim 30, wherein the GUI comprises~~ A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information including a Plot window for enabling the user to select a signal at a specific time cycle from the waveform of the signal displayed to the user;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules.

37. (Currently Amended) A system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information;

b. an Analysis Region Selection tool for selecting an analysis region for verifying the circuit design;

c. a Formal Verification tool for verifying the circuit design using the selected analysis region and ~~the~~ verified user defined rules;

d. a Productivity Choice Determination tool to determine high-productivity choices for expanding the analysis region if verification fails;

e. an Articulation Point Selection tool to identify ~~the~~ articulation points corresponding to the analysis region to choose smaller analysis region for circuit verification;

f. a Rule Verifier for verifying user defined rules for the analysis region; and

g. a database for storing a set of triples based on a set of signals selected by the user.

38. (Cancelled)

39. (Cancelled)

40. (Cancelled)

Please cancel claims 1-5, 7, 10, 12, 15, 21, 30, and 38-40 without prejudice or disclaimer